Conventional computer chips are designed for synchronous operation, which means that a square wave “clock” signal synchronizes the switching operation of the transistors. The operation speed of the computer is therefore directly related to the speed of the clock signal. Synchronous design has some advantages; however, one major disadvantage is that substantially more power is required to operate the system versus asynchronous, clockless design.

For a single computer being powered from the commercial electric power grid, power consumption is not a major consideration. However, for an application where the computer must be operated on battery power, the life of the battery is directly affected by the power draw of the device. Cell phones, hand-held computer devices, and computers on satellites and in remote areas of the planet, must by necessity be operated on batteries; and when these batteries have given up all of their power, they must be re-charged before the computer can continue to operate. It has long been known that asynchronous chip designs require less power than synchronous ones; however, many theoretical and practical problems have prevented widespread usage of asynchronous design methodologies in the semiconductor industry.

Now, a new design methodology for producing practical asynchronous computer chips using an industry-standard CAD tool flow has been developed. The resulting power usage of these asynchronous chips is less than 40% of the power used by their synchronous counterparts for the same application operating at the same speed. Additionally, these asynchronous circuits dynamically adjust to reductions in the supply voltage, such that they continue to operate correctly even when battery charge is extremely low.

This new asynchronous circuit design technology is available for license from the University of Arkansas.

For more information:  Mark Swaney
mswaney@uark.edu or 479-575-7243
http://www.uark.edu/ua/techip
Ref.: 10-01
8/13/09